10/737058

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: James W. NICHOLES

Assignee: Freescale Semiconductor, Inc.

Title: LOW-POWER COMPILER-PROGRAMMABLE MEMORY WITH FAST ACCESS TIMING

Patent No.: 7,050,354 B2 Issued: May 23, 2006

Atty. Docket No.: 1280-SC12980TC

MS: Certificate of Correction Branch
COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, VA 22313-1450

**REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT—
PTO MISTAKE (37 C.F.R. § 1.322(a))**

Dear Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322(a), please issue a Certificate of Correction in the above-identified matter. The mistake(s) to be corrected was made by the Office.

1. Attached hereto, in duplicate, is Form PTO-1050, with at least one copy suitable for printing.
2. The exact page(s) and line number(s) where the error(s) is shown correctly in the application file: Response to Office Action dated November 25, 2005, pages 3, 5, 6 and 7
3. Please send the Certificate to:

   J. GUSTAV LARSON
   LARSON NEWMAN ABEL POLANSKY & WHITE, LLP
   5914 WEST COURTYARD DRIVE, SUITE 200
   AUSTIN, TEXAS 78730

Respectfully submitted,

6-16-06
Date

/J. Gustav Larson/
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PTO/SB/44 (05-03)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,050,354 B2

DATED : May 23, 2006

INVENTOR(S) : James W. Nicholes

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column No. 9, Line No. 50 change "methods" to --method,--

Column No.10, Line No. 48 change "alter" to --after--

Column No. 10, Line No. 52 change "to" to --the--

Column No. 10, Line No. 62 change "to" to --the--

Column No. 11, Line No. 20 change "sense" to --sensed--

Column No. 12, Line No. 37 change "clinging" to --charging--

MAILING ADDRESS OF SENDER:
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PATENT NO.: 7,050,354 B2

No. of additional copies

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PATENT NO.: 7,050,354 B2

No. of additional copies

JUN 26 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	James Nicholes		
Title:	LOW-POWER COMPILER- PROGRAMMABLE MEMORY WITH FAST ACCESS TIMING		
App. No.:	10/737,058	Filed:	December 16, 2003
Examiner:	Tan Nguyen	Group Art Unit:	2827
Atty. Dkt. No.:	1280-SC12980TC		

Mail Stop AMENDMENT
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Dear Sir:

In response to the Office Action mailed October 19, 2005, please amend the above-identified application as follows:

Claim Amendments begin on page 2.

Remarks begin on page 8.

CERTIFICATE OF TRANSMISSION/MAILING
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to the Commissioner for Patents on 11/25/05.

Ryan Davidson
Typed or Printed Name

Signature

CLAIM AMENDMENTS

Please amend claims 1 and 5 as indicated in the following.

Please cancel claim 4 without prejudice or disclaimer as indicated in the following.

Claims Listing:

1. (Currently Amended) A method comprising:
discharging a plurality of bit lines during an inactive memory access period;
applying a charging pulse on a select one of the plurality of bit lines; and
after applying the charging pulse, waiting a delay time before sensing a voltage difference between the select one of the plurality of bit lines and a reference line, the delay time sufficient to allow the select one of the plurality of bit lines to be pulled towards a voltage level corresponding to a stored value in a selected memory bit cell.

2. (Previously Presented) The method, as recited in Claim 1,wherein the charging pulse has a width and the sensing occurs during a delay after the charging pulse, wherein the width and the delay are determined according to a size of a memory.

3. (Previously Presented) The method, as recited in Claim 1, wherein the charging pulse has a width and the sensing occurs during a delay after the charging pulse, wherein the memory is a compilable memory and the width and the delay are calculatable according to a selectable size of a memory.

4. (Canceled)

5. (Currently Amended) ~~The method, as recited in Claim 1, further comprising:~~ A method comprising:

discharging a plurality of bit lines during an inactive memory access period;

applying a charging pulse on a select one of the plurality of bit lines; and

after applying the charging pulse, waiting a delay time before sensing [[the]]a voltage difference between the select one of the plurality of bit lines and the reference line, the delay time sufficient to allow the reference line to be pulled towards a reference voltage

6. (Previously Presented) The method, as recited in Claim 1, wherein the voltage difference is greater than or equal to 100 millivolts.

7. (Currently Amended) The method, as recited in Claim 1, wherein the voltage difference is greater than or equal to 150 millivolts.

8. (Original) The method, as recited in Claim 1, further comprising:

applying another charging pulse on the reference line.

9. (Original) The method, as recited in Claim 1, further comprising:

discharging the reference line during the inactive memory access period.

10. (Original) The method, as recited in Claim 1, wherein applying the charging pulse on the select one of the plurality of bit lines draws a voltage of the select one of the plurality of bit lines to a midpoint voltage level.

11. (Original) The method, as recited in Claim 1, further comprising:

applying a charging pulse on the reference line, wherein applying the charging pulse on the reference lines draws a voltage of the reference line to a midpoint voltage level.

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12. (Original) The method, as recited in Claim 1, wherein after applying the charging pulse on the select one of the plurality of bit lines and before sensing the voltage difference, a voltage of the select one of the plurality of bit lines is drawn to a voltage level by a stored value in a selected memory bit cell.

13. (Previously Presented) A memory array comprising:

a plurality of bit lines;

a plurality of discharge transistors, each of the plurality of discharge transistors coupled one-to-one to a corresponding bit line of the plurality of bit lines, wherein the plurality of discharge transistors are configured to discharge the plurality of bit lines to a logic low during an inactive memory access period, wherein a selected discharge transistor of the plurality of discharge transistors is configured to stop discharging a selected bit line of the plurality of bit lines during an active memory access period;

a plurality of passgate transistors configured as a multiplexer, each of the plurality of passgate transistors coupled one-to-one to the corresponding bit line of the plurality of bit lines, the plurality of passgate transistors configured to select one of the plurality of bit lines as a sensed node; and

a pull-up transistor coupled to the sensed node, the pull-up transistor configured to provide a charging pulse to the sensed node upon entering the active memory access period.

14. (Original) The memory array, as recited in Claim 13, further comprising:

a sense amplifier coupled to the sensed node and a reference node, the sense amplifier configured to sense a difference between a voltage level on the sensed node and a voltage level on the reference node.

15. (Original) The memory array, as recited in Claim 14, wherein the difference is at least 100 millivolts.

16. (Previously Presented) The memory array, as recited in Claim 14, wherein the charging pulse has a width, wherein the sense amplifier is configured to sense the difference during a delay period after the charging pulse, and wherein the width and the delay period are determined according to a size of the memory array.

17. (Previously Presented) The memory array, as recited in Claim 14, wherein the charging pulse has a width, wherein the sense amplifier is configured to sense the difference during a delay period after the charging pulse, and wherein the memory array is a compilable memory and the width and the delay are calculatable according to a selectable physical size of the memory array.

18. (Original) The memory array, as recited in Claim 17, further comprising:

a pulse width selectable delay unit, wherein the pulse width selectable delay unit is configured to produce the delay period by selecting one or more units of pulse delay devices according to a mathematical equation based on the selectable size of the memory array; and

a delay period selectable delay unit, wherein the delay period selectable delay unit is configured to produce the delay period by selecting one or more units of period delay devices according to the mathematical equation.

19. (Previously Presented) The memory array, as recited in Claim 14, wherein the charging pulse has a width, wherein the sense amplifier is configured to sense the difference during a delay period after the charging pulse, and wherein the delay period is sufficient to allow the sensed node to be pulled towards a voltage level corresponding to a stored value in a selected memory bit cell of the memory array.

20. (Original) The memory array, as recited in Claim 14, further comprising:

reference circuitry configured to generate the reference node; wherein the reference circuitry is configured to discharge the reference node low during the inactive memory access period and provide another charging pulse to the sensed node upon entering the active memory access period..

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21. (Original) The memory array, as recited in Claim 13, wherein the pull-up transistor coupled to the sensed node draws a voltage of the sense node to a midpoint voltage level.

22. (Previously Presented) A circuit design tool comprising:

a compilable memory unit;

wherein a user can select a size of a memory unit to be included in a circuit design;

wherein the compilable memory unit comprises a set of instructions configured to:

calculate a delay period and a pulse width based on the size of the memory unit;

create the memory unit, wherein the memory unit comprises:

a plurality of bit lines;

a plurality of discharge transistors, each of the plurality of discharge transistors coupled to a corresponding one of the plurality of bit lines, wherein the plurality of discharge transistors are configured to discharge the plurality of bit lines to a logic low during an inactive memory access period, wherein a selected discharge transistor of the plurality of discharge transistors is configured to stop discharging a selected bit line of the plurality of bit lines during an active memory access period;

a plurality of passgate transistors configured as a multiplexer, a respective one of the plurality of passgate transistors coupled to each of the plurality of bit lines, the plurality of passgate transistors configured to select one of the plurality of bit lines as a sensed node; and

a pull-up transistor coupled to the sensed node, the pull-up transistor configured to provide a charging pulse having the pulse width to the sensed node upon entering the active memory access period.

23. (Previously Presented) The circuit design tool, as recited in Claim 22, wherein the memory unit further comprises:

a sense amplifier coupled to the sensed node, the sense amplifier configured to sense a difference between a voltage level on the sensed node and a voltage level on a reference node during the delay period after the charging pulse.

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24. (Previously Presented) A circuit design tool comprising:

a compilable memory unit;

wherein a user can select a size of a memory unit to be included in a circuit design;

wherein the compilable memory unit comprises a set of instructions configured to:

calculate a delay period and a pulse width based on the size of the memory unit;

provide the memory unit;

wherein the memory unit is configured to:

discharge a plurality of bit lines during an inactive memory access period;

apply a charging pulse on a select one of the plurality of bit lines; and

sensing a voltage difference between the select one of the plurality of bit lines and a reference line;

wherein the charging pulse has a width of the pulse width and the sensing occurs during the delay period after the charging pulse.

JUN 26 2006

REMARKS

The Office Action dated October 19, 2005 has been received and considered. In this response, claims 1 and 5 have been amended and claim 4 has been canceled without prejudice or disclaimer. Support for the amendments may be found in the specification and drawings as originally filed. Reconsideration of the outstanding rejections in the present application is respectfully requested based on the following remarks.

Allowability of Claims 2-5 and 13-24

The Applicant notes with appreciation the indication that claims 13-24 are allowed and claims 2-5 would be allowable if rewritten in independent form. In the interest of advancing the present application to issuance, claim 1 has been amended to include the features recited by allowable claim 4 and claim 5 has been rewritten in independent form. It is respectfully submitted that claims 1 and 5, as well as dependent claims 2, 3, and 6-12, are allowable at least for the same reasons indicated by the Office Action.

Obviousness Rejection of Claims 1 and 6-12

At page 2 of the Office Action, claims 1 and 6-12 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kohno (U.S. Patent No. 5,703,820). As noted above, claim 1 has been amended to recite the additional features recited by allowable claim 4, thereby obviating this rejection. Reconsideration and withdrawal of this rejection therefore is respectfully requested.

Conclusion

The Applicant respectfully submits that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

2006

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

25 November 2005
Date

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